

APPLICATION
FOR
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Title:

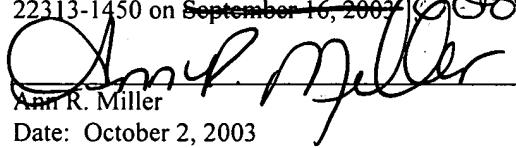
EMC Immunity Improvements to USB Interface

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AXIOHM TRANSACTION SOLUTIONS, INC.

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Patent Application Of: Randolph A. Bullock and James R. Del Signore II

For: EMC Immunity Improvements to USB interface

BACKGROUND OF THE INVENTION

1. Field of Invention

[001] The present invention relates to hardware designed for electromagnetic compatibility (EMC) immunity and, more specifically, to a standard Universal Serial Bus (USB) interface having improved EMC.

2. Description of Prior Art

[002] Universal Serial Bus, or USB, architecture is becoming a popular substitute for parallel or serial bus architecture, and USB ports, in addition to parallel and serial ports, are provided as standard equipment on most computers manufactured today. USB specifications are available at the URL <http://www.usb.org>.

[003] USB requires a single pair of twisted wires in a cable for data transmission, while a second pair provides power from a host to a peripheral unit. Three signaling conditions are utilized. Data packets are sent using differential signaling followed by an end of packet, where both lines go low for two clocks. A third state is the idle state where neither line is driven, but one is pulled up by a resistor at the device end. The host controls the packet flow such that when the peripheral is sending data, the host is in receive mode, and vice-versa, and no collisions are possible.

[004] While the USB interface has brought more flexibility, packetized data integrity, and automatic configuration to PC-connected peripherals, the interface defined by the USB - Integrator's Forum (USB-IF) has inherent deficiencies in meeting today's European Norm (EN) EMC immunity requirements. Although the published USB standards (Rev. 1.1 or 2.0) require all devices bearing the USB logo to meet today's EN requirements for "CE" mark, very few commercially available USB peripherals actually do so on the immunity side. The forum for acceptance of USB devices, known as "Plugfest," focuses primarily on the functional aspects of

compliance to the USB standard in terms of link level protocols and signal integrity, neglecting the CE mark EMC requirements invoked in the USB standard.

[005] Under the broad term EMC Immunity, as defined in EN55024, are specific tests such as ESD, EFT, RFI, and CRFI that apply and are required to meet CE mark. In particular peripheral markets, namely peripherals for use in a point of sale environment, such as POS-printers, the standard CE mark tests are required, but at higher voltage treatment levels. As such, EMC immunity can quickly become the major obstacle in the use of USB in a POS environment. Due to these higher level Immunity requirements, POS has been accurately depicted as an industrial level of Immunity.

[006] In terms of ESD immunity, because the USB device controller is connected to the physical interface conductors and contains RAM registers that can be easily upset by large ESD-induced signal transients, immunity to ESD is inherently poor. In terms of EFT immunity, some of the same problems as with ESD are encountered, except that instead of altered logic states, either the Early End of Packet (Early EOP) or Babble are caused due to poor recovery mechanisms in the hardware.

[007] The reason these conditions are reached during EFT testing is an unlucky choice of Start Of Frame (SOF) packet interval at an exact harmonic of the likewise arbitrary pulse frequency chosen by the EFT committee as the basis for the EFT test. Without improving basic signal robustness or cabling, a choice of slightly different SOF interval would eliminate the chance of having several SOF packets in a row lost to interference during EFT testing. In fact, a 1 ms SOF interval ensures that eventually, up to 15 SOF in a row will be lost to a 15ms burst of 5KHz energy injected on either the signal cable or AC mains to the POS-device (i.e., printer) during the EFT test, which will likely result in a disconnected device having no fully USB-compliant method of automatic reconnection.

[0081] While use of common mode chokes are known to control fault currents in lower speed electronic interfaces, their use is expressly not recommended by the USB-IF in USB interfaces, presumably due to the topology and signaling methods used in USB.

3. **Objects and Advantages**

[009] It is therefore a principal object and advantage of the present invention to provide improved EMC immunity in a USB interface.

[010] It is an additional object and advantage of the present invention to provide improved EMC immunity while not degrading signal integrity.

[011] Other objects and advantages of the present invention will in part be obvious, and in part appear hereinafter.

SUMMARY OF THE INVENTION

[012] In accordance with the foregoing objects and advantages, the present invention provides a device for improving EMC immunity in a USB interface while maintaining the integrity of the signal. The invention generally comprises use of a common mode choke through which each of the USB's four signal lines pass. The choke operates by passing the signal lines through a common coupling ferrite core, allowing the fault current to pass by on the shield uninhibited while blocking common-mode currents with ferrite impedance much stronger than could be tolerated on each signal data line individually. In addition, bypass capacitors, such as Tantalum bypass capacitors, and a 5.6V Transorb device are added to the 5V power supply of the controller, and all unused pins are terminated to reduce unwanted ringing transients in the controller leadframe. In addition, small capacitors (within the capacitive loading specification allowed by the USB-IF) are positioned next to the IC on each data line. In an alternative embodiment, the D+, D-, and USB ground lines each pass through the choke, and the USB 5V line is AC coupled to the USB ground line outside the choke and routed through a high impedance into the circuit, although this structure would not be practical for bus-powered devices which would need all four lines to pass through the choke.

BRIEF DESCRIPTION OF THE DRAWINGS

[013] Fig. 1 is a schematic of a USB interface modified in accordance with the preferred embodiment of the present invention.

[014] Fig. 2 is a schematic of a USB interface modified in accordance with an alternate embodiment of the present invention.

DETAILED DESCRIPTION

[015] Referring now to the drawing figures in which like reference numerals refer to like parts throughout, there is seen a Universal Serial Bus (USB) interface, referred to generally by reference numeral 10, that includes a USB Serial Interface Engine/Controller 12 for controlling communications flowing between a host computer and a peripheral, such as a printer. Interface 10 additionally comprises a power supply 14, four signal lines 16, 18, 20, 22 designated D+, D-, USB5V, and USB ground, respectively, (D+ and D- being data carrying wires and USB 5V and USB ground providing power between the computer and peripheral), an 8-bit data bus 24, status pins 26, and miscellaneous bus control signals 28.

[016] Referring to Figure 1, interface 10 further comprises a choke 30, through which signal lines 16, 18, 20, and 22 pass for purposes of improving EMC immunity. Choke 30 preferably comprises a ferrite core with inductors positioned therein that permit the lines 16 - 22 to pass therethrough while neglecting shield and permitting fault currents to pass by on the shield uninhibited while blocking common mode currents with ferrite impedance much stronger than could be tolerated on each data line individually. Power source 14 contains bypass capacitors 32, such as Tantalum bypass capacitors, and a 5.6V transorb device 34. All unused pins 28 are terminated to reduce ringing transients in the controller lead frame.

[017] Referring to Figure 2, an alternate embodiment of interface 10 comprises a choke 30, through which signal lines 16, 18, and 22 pass. USB 5V line 20 is AC coupled to USB ground line 22 outside of choke 30 and routed through high impedance 36.

[018] As seen in Figs. 1 and 2, USB 5V line 20, the reset input, and strobe output 26, 28 are filtered by RC networks to prevent transients from inducing modified signal states in either the controller 12 or host microprocessor.